

NCP3065, NCV3065

MAXIMUM RATINGS (measured vs. pin 4, unless otherwise noted)

Rating	Symbol	Value	Unit
V _{CC} (Pin 6)	V _{CC}	0 to +40	V
Comparator Inverting Input (Pin 5)	V _{CI}	-0.2 to +V _{CC}	V
Darlington Switch Collector (Pin 1)	V _{SWC}	0 to +40	V
Darlington Switch Emitter (Pin 2) (Transistor OFF)	V _{SWE}	-0.6 to +V _{CC}	V
Darlington Switch Collector to Emitter (Pins 1-2)	V _{SWCE}	0 to +40	V
Darlington Switch Current	I _{SW}	1.5	A
I _{pk} Sense (Pin 7)	V _{IPK}	-0.2 to V _{CC} + 0.2	V
Timing Capacitor (Pin 3)	V _{TCAP}	-0.2 to +1.4	V

Power Dissipation and Thermal Characteristics

PDIP-8 (Note 5) Thermal Resistance Junction-to-Air	R _{θJA}	100	°C/W
SOIC-8 (Note 5) Thermal Resistance Junction-to-Air	R _{θJA}	180	°C/W
DFN-8 (Note 5) Thermal Resistance Junction-to-Air Thermal Resistance Junction-to-Case	R _{θJA} R _{θJC}	78 14	°C/W
Storage Temperature Range	T _{STG}	-65 to +150	°C
Maximum Junction Temperature	T _{J(MAX)}	+150	°C
Operating Junction Temperature Range (Note 3) NCP3065, NCV3065	T _J	-40 to +125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- This device series contains ESD protection and exceeds the following tests:
Pin 1-8: Human Body Model 2000 V per AEC Q100-002; 003 or JESD22/A114; A115
Machine Model Method 200 V
- This device contains latch-up protection and exceeds 100 mA per JEDEC Standard JESD78.
- The relation between junction temperature, ambient temperature and Total Power dissipated in IC is $T_J = T_A + R_{\theta} \cdot P_D$
- The pins which are not defined may not be loaded by external signals
- 1 oz copper, 1 in² copper area

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ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise specified)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
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OSCILLATOR

Frequency	(VPin 5 = 0 V, CT = 2.2 nF, $T_J = 25^\circ\text{C}$)	f_{OSC}	110	150	190	kHz
Discharge to Charge Current Ratio	(Pin 7 to V_{CC} , $T_J = 25^\circ\text{C}$)	I_{DISCHG} / I_{CHG}	5.5	6.0	6.5	–
Capacitor Discharging Current	(Pin 7 to V_{CC} , $T_J = 25^\circ\text{C}$)	I_{DISCHG}		1650		μA
Capacitor Charging Current	(Pin 7 to V_{CC} , $T_J = 25^\circ\text{C}$)	I_{CHG}		275		μA
Current Limit Sense Voltage	($T_J = 25^\circ\text{C}$) (Note 7)	$V_{IPK(Sense)}$	165	185	235	mV

OUTPUT SWITCH (Note 6)

Darlington Switch Collector to Emitter Voltage Drop	($I_{SW} = 1.0\text{ A}$, $T_J = 25^\circ\text{C}$) (Note 6)	$V_{SWCE(DROP)}$		1.0	1.3	V
Collector Off-State Current	($V_{CE} = 40\text{ V}$)	$I_{C(OFF)}$		0.01	100	μA

COMPARATOR

Threshold Voltage	$T_J = 25^\circ\text{C}$	V_{TH}		235		mV
	$T_J = 0$ to $+85^\circ\text{C}$			± 5		%
	$T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$	V_{TH}	-10		+10	%
Threshold Voltage Line Regulation	($V_{CC} = 3.0\text{ V}$ to 40 V)	REG_{LINE}	-6.0		6.0	mV
Input Bias Current	($V_{in} = V_{th}$)	$I_{CII\ in}$	-1000	-100	1000	nA

TOTAL DEVICE

Supply Current	($V_{CC} = 5.0\text{ V}$ to 40 V , CT = 2.2 nF, Pin 7 = V_{CC} , VPin 5 > V_{th} , Pin 2 = GND, remaining pins open)	I_{CC}			7.0	mA
Thermal Shutdown Threshold				160		$^\circ\text{C}$
Hysteresis				10		$^\circ\text{C}$

6. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
7. The $V_{IPK(Sense)}$ Current Limit Sense Voltage is specified at static conditions. In dynamic operation the sensed current turn-off value depends on comparator response time and di/dt current slope. See the Operating Description section for details.
8. NCV prefix is for automotive and other applications requiring site and change control.

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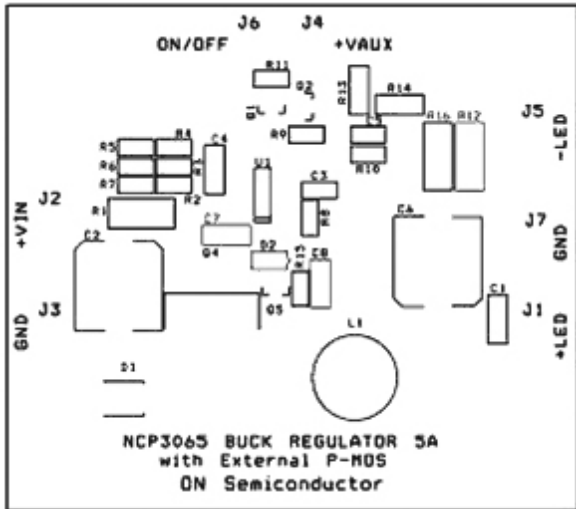


Figure 26. 3 A Buck Demoboard Layout

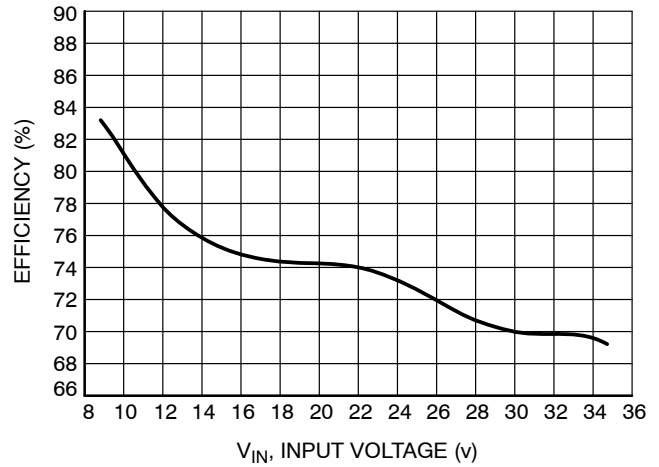


Figure 27. Efficiency vs. Input Voltage for the 3 A Buck Demo Board at $I_{OUT} = 3\text{ A}$, $V_{OUT} = 4\text{ V}$, $T_A = 25^\circ\text{C}$

ORDERING INFORMATION

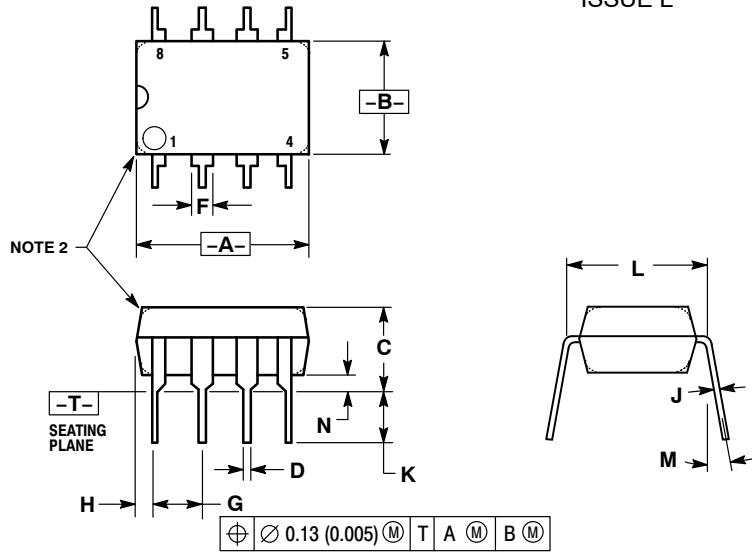
Device	Package	Shipping [†]
NCP3065MNTXG	DFN-8 (Pb-Free)	4000 Units / Tape & Reel
NCP3065PG	PDIP-8 (Pb-Free)	50 Units / Rail
NCP3065DR2G	SOIC-8 (Pb-Free)	2500 Units / Tape & Reel
NCV3065MNTXG	DFN-8 (Pb-Free)	4000 Units / Tape & Reel
NCV3065PG	PDIP-8 (Pb-Free)	50 Units / Rail
NCV3065DR2G	SOIC-8 (Pb-Free)	2500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

8 LEAD PDIP
CASE 626-05
ISSUE L



NOTES:

1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

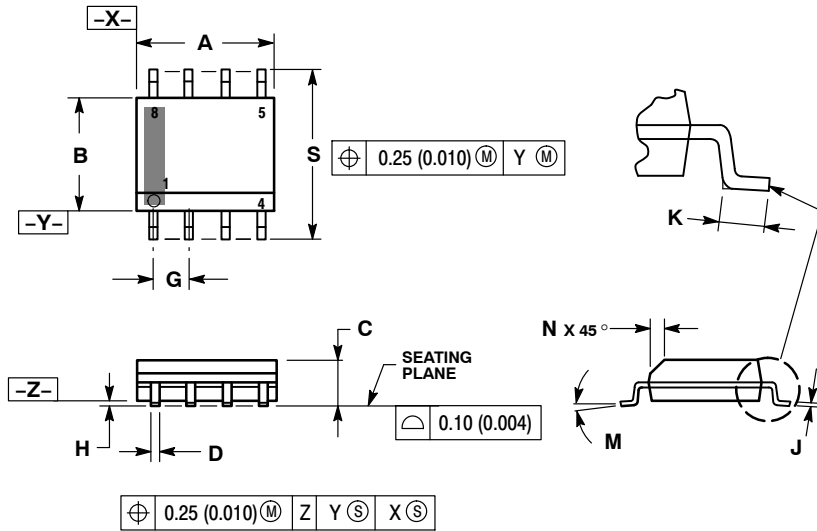
STYLE 1:

- PIN 1. AC IN
- DC + IN
- DC - IN
- AC IN
- GROUND
- OUTPUT
- AUXILIARY
- V_{CC}

NCP3065, NCV3065

PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE AH

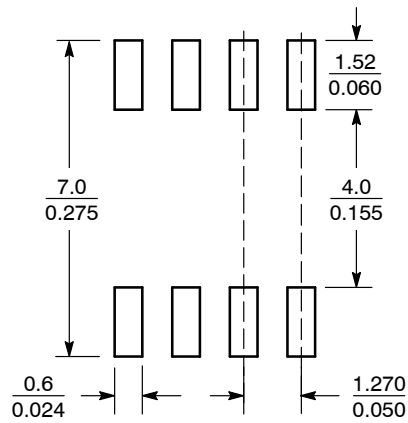


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.